CLAIMS

What is claimed is:

1. A chip comprising:

a transmitter including a cycle encoding circuit to receive a data input signal and to provide a full cycle encoded signal in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals, and wherein data is represented in data time segments of the full cycle encoded signal and no data time segment has more than one cycle of an encoding signal.

2. The chip of claim 1, wherein the transmitter further includes a complementary cycle encoding circuit to receive the data input signal and to provide a complementary full cycle encoded signal in response thereto.

3. The chip of claim 1, wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input signal and which encoding signal was selected for a previous data time segment.

4. The chip of claim 1, further comprising a periodic signal source to provide a periodic reference signal and wherein the transmitter includes circuits to provide the encoding signals in response to the periodic reference signal.

5. The chip of claim 4, wherein the periodic reference signal has period that is equal to the time length of the data time segments.

6. The chip of claim 4, wherein the periodic reference signal has a period that is equal to the time length of a data bit cell of the data input signal.

7. The chip of claim 1, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

8. The chip of claim 1, wherein the full cycle encoded signal represents a 0 or a 1 depending on the value of the data.

9. The chip of claim 1, further comprising a receiver that includes an initial receiving circuit, a delay circuit and a logic circuit to provide a data out signal which recovers data from another full cycle encoded signal.

10. A chip comprising:

a transmitter including a cycle encoding circuit to receive a data input signal and a periodic reference signal and to provide a cycle encoded signal in response thereto, wherein in response to the data input signal and a periodic reference signal, the cycle encoded signal is formed of continuously joined portions of encoding signals during successive data time segments, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals.

11. The chip of claim 10, wherein the cycle encoded signal is a full cycle encoded signal in which no data time segment has more than one cycle of an encoding signal.

12. The chip of claim 10, wherein the transmitter further includes a complementary cycle encoding circuit to receive the data input signal and the periodic reference signal and to provide a complementary cycle encoded signal in response thereto, wherein the complementary cycle encoded signal is a logical inverse of the cycle encoded signal.

13. The chip of claim 10, wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the cycle encoded signal in response to the data input signal and which encoding signal was selected for a previous data time segment.

14. The chip of claim 10, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

15. The chip of claim 10, further comprising a receiver that includes an initial receiving circuit, a delay circuit and a logic circuit to provide a data out signal which recovers data from another cycle encoded signal.

16. A system comprising:

a transmitter including a cycle encoding circuit to receive a data input signal and to provide a full cycle encoded signal in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals, and wherein data is represented in data time segments of the full cycle encoded signal and no data time segment has more than one cycle of an encoding signal; and

a receiver to receive the full cycle encoded signal and recover values of the data input signal in response thereto.

17. The system of claim 16, wherein the transmitter further includes a complementary cycle encoding circuit to receive the data input signal and to provide a complementary full cycle encoded signal in response thereto.

18. The system of claim 16, wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the full cycle encoded signal in response to the data input signal and which encoding signal was selected for a previous data time segment.

19. The system of claim 16, further comprising a periodic signal source to provide a periodic reference signal and wherein the transmitter includes circuits to provide the encoding signals in response to the periodic reference signal.

20. The system of claim 16, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

21. The system of claim 16, wherein the receiver that includes an initial receiving circuit, a delay circuit and a logic circuit to provide a data out signal which includes the recovered values of the data input signal.

22. The system of claim 21, wherein the recovered values are the inverse of those of the data input signal.

23. A system comprising:

a transmitter including:

(a) a cycle encoding circuit to receive a data input signal and to provide a cycle encoded signal in response thereto by continuously joining portions of different encoding signals, wherein some of the encoding signals have a different frequency than others of the encoding signals and some of the encoding signals have a different phase than others of the encoding signals; and

(b) a complementary cycle encoding circuit to receive the data input signal and to provide a complementary cycle encoded signal in response thereto by continuously joining portions of the different encoding signals; and

a receiver to receive the cycle encoded signal and the complementary cycle encoded signal and to recover values of the data input signal in response thereto.

24. The system of claim 23, wherein the cycle encoding circuit includes a multiplexer to receive the data input signal and the encoding signals and to select the portions of the encoding signals that are to form the cycle encoded signal in response to the data input signal and which encoding signal was selected for a previous data time segment.

25. The system of claim 23, further comprising a periodic signal source to provide a periodic reference signal and wherein the transmitter includes circuits to provide the encoding signals in response to the periodic reference signal.

26. The system of claim 23, wherein the encoding signals include a first signal with frequency F, a second signal that is an inverse of the first signal, a third signal that has a frequency F/2, and a fourth signal that is an inverse of the third signal.

27. The system of claim 23, wherein the receiver that includes an initial receiving circuit, a delay circuit and a logic circuit to provide a data out signal which includes the recovered values of the data input signal.

28. The system of claim 23, wherein the cycle encoded signal is a full cycle encoded signal in which no data time segment has more than one cycle of an encoding signal.